TSD2Q-PCN-xxC

800G OSFPDD TO 2x400G QSFP112 Direct Attach Cable

Description

QSFP-DD (Double Density) Interconnect System and Cable Assemblies feature an eight-lane electrical interface that transmits up to 112Gbps PAM-4,up to 800Gbps aggregate. QSFP-DD offers the same footprint as QSFP interconnects, making them backward compatible. The double density feature is an extended paddle card with two rows of high-speed context.

400G QSFP112 passive cable assembly products, based on 4X100G or 4X112G structure, this product can well meet the next generation of 400G switches, servers, routers and other products application needs. The QSFP112 cable assembly is optimised to reduce crosstalk and insertion loss and has excellent signal integrity, fully compliant with the next generation 400G Ethernet standards.

Features

- MEET SFF-8432 & OSFP MSA
- MEET TO CMIS Rev5.1
- MEET IEEE802.3cd&IEEE802.3 ck
- Support I2C two - line string interface, easy to control
- Support for hot plugging
- Low crosstalk
- Eight-lane electrical interface transmits up to 112Gbps
- ROHS Compliance

Applications

- SWITCH/Router
- Data storage and communication industry
- Data center, cloud server

Recommended Operation Condition

Parameters	Symbol	Min.	Max.	Unit
Operating Case Temperature	Topc	0	70	degC
Storage Temperature	Tst	-40	85	degC
Relative Humidity (non-condensation)	RS	35	60	%
Supply Voltage	Vcc3	3.135	3.465	V
Voltage on LVTTL Input	Vilvttl	-0.3	Vcc3+0.2	V
Power Supply Current	Icc3	-	15	mA
Total Power Consumption	Pd	-	0.05	W

Notes:

Stress or conditions exceed the above range may cause permanent damage to the device.

This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not applied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

High Speed Characteristics

Item		Requirement	Test Condition
Differential Impedance	Cable Impedance	100±5Ω	Rise time of 25ps (20 % - 80 %)
	Paddle Card Impedance	100±10Ω	
	Cable Termination Impedance	100±10Ω	
Differential (Input/Output)Return loss S_{DD11}/S_{DD22}		Return_loss(f)≥ $\begin{cases} 16.5-2\sqrt{f} & 0.05\le f < 4.1 \\ 10.66-14\log_{10}(f/5.5) & 4.1\le f\le 40 \end{cases}$ Where f is the frequency in GHz Return loss(f) is the return loss at frequency f	10MHz≤f≤40GHz
Differential to common-mode (Input/Output)Return loss S_{CD11}/S_{CD22}		Return_loss(f)≥ $\begin{cases} 22-10(f/26.56) & 0.05\le f < 26.56 \\ 15-3(f/26.56) & 26.56\le f\le 40 \end{cases}$ Where f is the frequency in GHz Return_loss(f) is the Differential to common-mode return loss at frequency f	50MHz≤f≤40GHz
Common-mode to Common-mode (Input/Output)Return loss S_{CC11}/S_{CC22}		Return_loss(f)≥1.8dB 0.05≤f≤40 Where f is the frequency in GHz Return_loss(f) is the Differential to common-mode return loss at frequency f	50MHz≤f≤40GHz
Differential Insertion Loss (S_{DD21} Max.)		(Differential InsertionLoss Max. For TPa to TPb Excluding Test fixture)	50MHz≤f≤40GHz
		Insertion _loss(f)≥-19.75dB 0.05≤f≤26.56 Where f is the frequency in GHz Insertion Loss (f) Differential Insertion Loss at frequency f	
Insertion Loss Deviation		-0.176*f - 0.7 ≤ ILD ≤ 0.176* f + 0.7	50MHz≤f≤26.56GHz

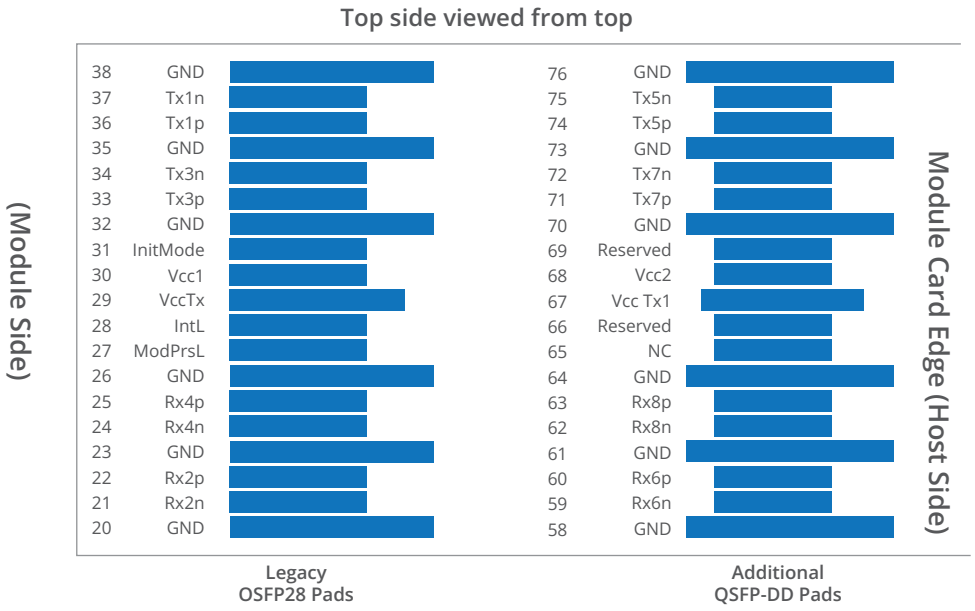
Differential to common-mode Conversion Loss-Differential Insertion Loss(S_{CD21}-S_{DD21})	Conversion _loss(f) – IL(f)≥ $\begin{cases} 10 & 0.05 \le f < 12.89 \\ 14-0.3108f & 12.89 \le f < 40 \end{cases}$ Where f is the frequency in GHz Conversion_loss(f) is the cable assembly differential to common-mode conversion loss IL(f) is the cable assembly insertion loss	50MHz≤f ≤40GHz
MDNEXT(multiple disturber near-end crosstalk)	≥35dB @26.5GHz	10MHz≤f ≤26.5GHz
Intra Skew	10ps/m,	10MHz≤f ≤26.5GHz

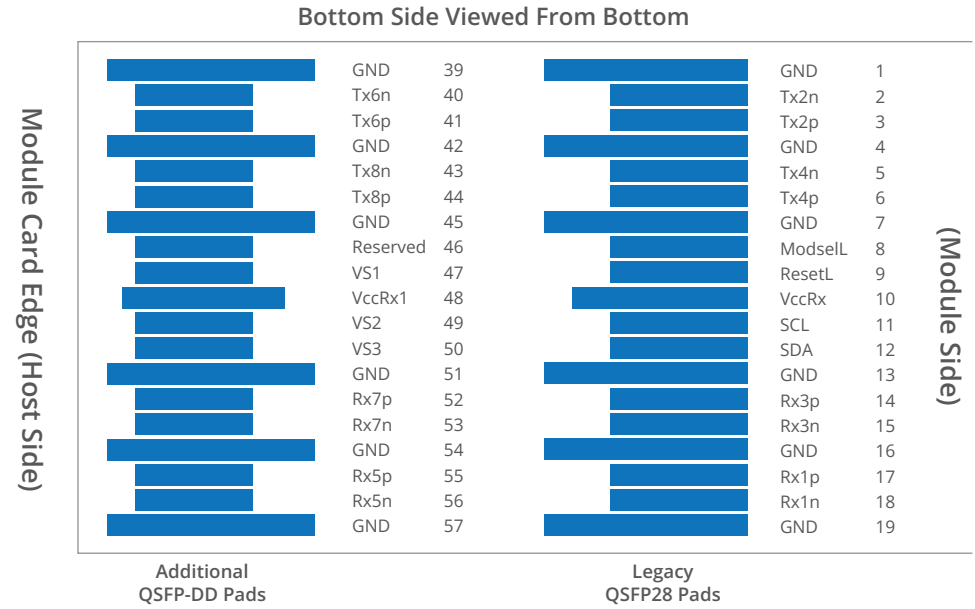
Pin Definition

Pin	Logic	Symbol	Name/Description
1	-	GND	Ground
2	CML-I	Tx2n	Transmitter inverted data input
3	CML-I	Tx2p	Transmitter non-inverted data input
4	-	GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7	-	GND	Ground
8	LVTTL-I	MODSEIL	Module Select
9	LVTTL-I	ResetL	Module Reset
10	-	VCCRx	+3.3V Receiver Power Supply
11	LVCMOS-I/O	SCL	2-wire serial interface clock²
12	LVCMOS-I/O	SDA	2-wire serial interface data²
13	-	GND	Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16	-	GND	Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver inverted data output
19	-	GND	Ground
20	-	GND	Ground
21	CML-O	Rx2p	Receiver Inverted Data Output
22	CML-O	Rx2n	Receiver Non-Inverted Data Output
23	-	GND	Ground
24	CML-O	RX4p	Receiver Inverted Data Output
25	CML-O	RX4n	Receiver Non-Inverted Data Output
26	-	GND	Ground
27	LVTTL-O	ModPrsL	Module Present

28	LVTTL-O	IntL	Interrupt
29	-	Vcc Tx	+3.3V Transmitter Power Supply
30	-	Vcc1	+3.3V Power Supply
31	LVTTL-I	LPMode	Low Power Mode
32	-	GND	Ground
33	CML-I	Tx3p	Transmitter non-inverted data input
34	CML-I	Tx3n	Transmitter inverted data input
35	-	GND	Ground
36	CML-I	Tx1p	Transmitter non-inverted data input
37	CML-I	Tx1n	Transmitter non-inverted data input
38	-	GND	Ground
39	-	GND	Ground
40	CML-I	Tx6n	Transmitter inverted data input
41	CML-I	Tx6p	Transmitter non-inverted data input
42	-	GND	Ground
43	CML-I	Tx8n	Transmitter inverted data input
44	CML-I	Tx8p	Transmitter non-inverted data input
45	-	GND	Ground
46	-	Reserved	-
47	-	VS1	-
48	-	VCCRx1	+3.3V Power Supply
49	-	VS2	-
50	-	VS3	-
51	-	GND	Ground
52	CML-O	Rx7p	Receiver non-inverted data output
53	CML-O	Rx7n	Receiver inverted data output
54	-	GND	Ground
55	CML-O	Rx5p	Receiver non-inverted data output
56	CML-O	Rx5n	Receiver inverted data output
57	-	GND	Ground
58	-	GND	Ground
59	CML-O	Rx6n	Receiver inverted data output
60	CML-O	Rx6p	Receiver non-inverted data output
61	-	GND	Ground
62	CML-O	Rx8n	Receiver inverted data output
63	CML-O	Rx8p	Receiver non-inverted data output
64	-	GND	Ground
65	-	NC	-
66	-	Reserved	-
67	-	VccTx1	+3.3V Power Supply

68	-	Vcc2	+3.3V Power Supply
69	-	Reserved	-
70	-	GND	Ground
71	CML-I	Rx7p	Transmitter non-inverted data input
72	CML-I	Rx7n	Transmitter inverted data input
73	-	GND	Ground
74	CML-I	Tx5p	Transmitter non-inverted data input
75	CML-I	Tx5n	Transmitter inverted data input
76	-	GND	Ground





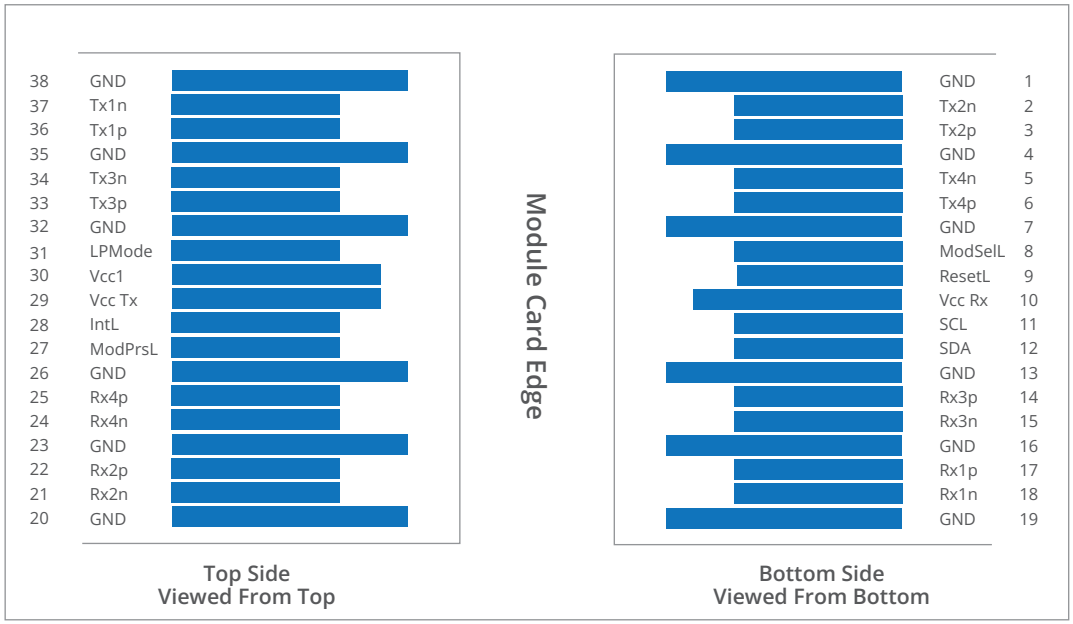
13	GND	Ground
14	Rx3p	Receiver Non-Inverted Data Output
15	Rx3n	Receiver Inverted Data Output
16	GND	Ground
17	Rx1p	Receiver Non-Inverted Data Output
18	Rx1n	Transmitter Inverted DATA in. AC Coupled
19	GND	Ground
20	GND	Ground
21	Rx2n	Receiver Inverted Data Output
22	Rx2p	Receiver Non-Inverted Data Output
23	GND	Ground
24	Rx4n	Receiver Inverted Data Output
25	Rx4p	Receiver Non-Inverted Data Output
26	GND	Ground
27	ModPrsL	Module Present
28	IntL	Interrupt
29	Vcc Tx	+3.3V Power supply transmitter
30	Vcc1	+3.3V Power Supply
31	LPMode	Low Power Mode
32	GND	Ground
33	Tx3p	Transmitter Non-Inverted Data Input
34	Tx3n	Transmitter Inverted Data Input
35	GND	Ground
36	Tx1p	Transmitter Non-Inverted Data Input
37	Tx1n	Transmitter Inverted Data Input
38	GND	Ground

Pin definition @QSFP

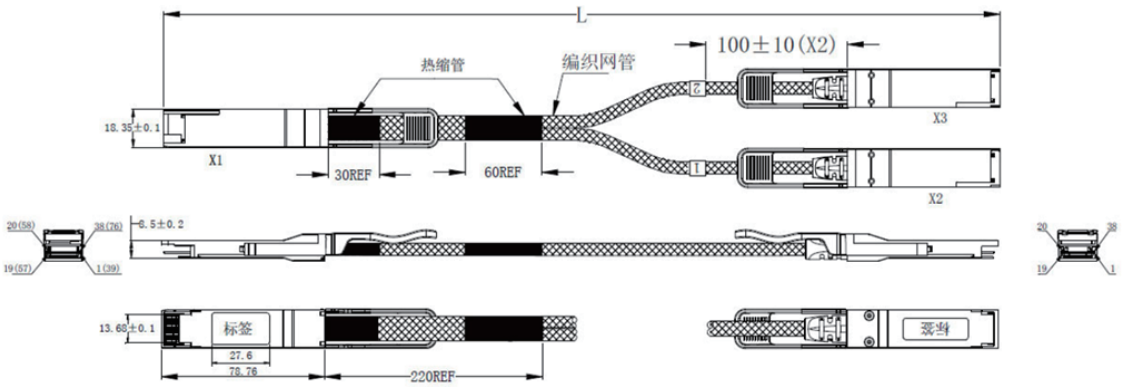
Pin	Symbol	Name/Description
1	GND	Ground
2	Tx2n	Transmitter Inverted Data Input
3	Tx2p	Transmitter Non-Inverted Data Input
4	GND	Ground
5	Tx4n	Transmitter Inverted Data Input
6	Tx4p	Transmitter Non-Inverted Data Input
7	GND	Ground
8	ModSelL	Module Select
9	ResetL	Module Reset
10	Vcc Rx	+3.3V Power supply receiver

11	SCL	2-wire serial interface clock
12	SDA	2-wire serial interface data
13	GND	Ground
14	Rx3p	Receiver Non-Inverted Data Output
15	Rx3n	Receiver Inverted Data Output
16	GND	Ground
17	Rx1p	Receiver Non-Inverted Data Output
18	Rx1n	Transmitter Inverted DATA in. AC Coupled
19	GND	Ground
20	GND	Ground
21	Rx2n	Receiver Inverted Data Output
22	Rx2p	Receiver Non-Inverted Data Output
23	GND	Ground
24	Rx4n	Receiver Inverted Data Output
25	Rx4p	Receiver Non-Inverted Data Output
26	GND	Ground
27	ModPrsL	Module Present
28	IntL	Interrupt
29	Vcc Tx	+3.3V Power supply transmitter
30	Vcc1	+3.3V Power Supply
31	LPMode	Low Power Mode
32	GND	Ground
33	Tx3p	Transmitter Non-Inverted Data Input
34	Tx3n	Transmitter Inverted Data Input
35	GND	Ground
36	Tx1p	Transmitter Non-Inverted Data Input
37	Tx1n	Transmitter Inverted Data Input
38	GND	Ground

Pin Descriptions @QSFP



Mechanical Specifications



Ordering Information

800G QSFPDD TO 2xQSFP112 Copper Cable Assemblies, Passive.

P/N	Length	Data Rate	AWG	Length Tolerance
TSD2Q-PCN-01C	1 m	800G	28/30	+3.5/-3.5 cm
TSD2Q-PCN-02C	2 m	800G	26/28	+3.5/-3.5 cm
TSD2Q-PCN-03C	3 m	800G	26	+3.5/-3.5 cm