TSD4Q-PCM-xxC

400Gbps QSFP DD To 4x QSFP56 Direct Attach Cable

Description

QSFP-DD (Double Density) Interconnect System and Cable Assemblies feature an eight-lane electrical interface that transmits up to 28Gbps NRZ or 56Gbps PAM-4, up to 200Gbps or 400Gbps aggregate. QSFP-DD offers the same footprint as QSFP interconnects, making them backward compatible. The double density feature is an extended paddle card with two rows of high-speed context. QSFP-DD meets IEEE 802.3bj, InfiniBand EDR, and SAS 3.0 specifications, allowing these connectors and cable assemblies to function across a variety of next-generation technologies and applications.

200G QSFP56 passive cable assembly products, based on 4X50G or 4X56G structure, this product can well meet the next generation of 200G switches, servers, routers and other products application needs. The QSFP56 cable assembly is optimised to reduce crosstalk and insertion loss and has excellent signal integrity, fully compliant with the next generation 200G Ethernet and InfiniBand HDR standards

Features

- MEET SFF-8636&QSFP-DD MSA
- MEET IEEE802.3bj&IEEE802.3 cd
- Support I2C two - line string interface, easy to control
- Support for hot plugging
- Low crosstalk
- Eight-lane electrical interface transmits up to 28Gbps NRZ or 56Gbps PAM-4

Applications

- Switches, servers and routers
- Data Center networks
- Storage area networks
- High performance computing
- Test and measurement equipment

Recommended Operation Condition

Parameters	Symbol	Min.	Max.	Unit
Operating Case Temperature	Topc	0	70	degC
Storage Temperature	Tst	-40	85	degC
Relative Humidity (non-condensation)	RS	35	60	%
Supply Voltage	Vcc3	3.135	3.465	V
Voltage on LVTTL Input	Vilvttl	-0.3	Vcc3+0.2	V
Power Supply Current	Icc3	-	15	mA
Total Power Consumption	Pd	-	0.05	W

Notes:

Stress or conditions exceed the above range may cause permanent damage to the device.

This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not applied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

High Speed Characteristics

<table>
<tr><th colspan="2">Item</th><th colspan="7">Requirement</th><th>Test Condition</th></tr>
<tr><td rowspan="3">Differential Impedance</td><td>Cable Impedance</td><td colspan="7">105+5/-10Ω</td><td rowspan="3">Rise time of 25ps
(20 % - 80 %)</td></tr>
<tr><td>Paddle Card Impedance</td><td colspan="7">100±10Ω</td></tr>
<tr><td>Cable Termination Impedance</td><td colspan="7">100±10Ω</td></tr>
<tr><td colspan="2">Differential (Input/Output)Return loss S_{DD11}/S_{DD22}</td><td colspan="7">Return_loss(f)≥ $\begin{cases} 16.5-2\sqrt{f} & 0.05\le f < 4.1 \\ 10.66-14\log_{10}(f/5.5) & 4.1\le f\le 19 \end{cases}$
Where f is the frequency in GHz
Return loss(f) is the return loss at frequency f</td><td>10MHz≤f ≤ 19GHz</td></tr>
<tr><td colspan="2">Differential to common-mode (Input/Output)Return loss S_{CD11}/S_{CD22}</td><td colspan="7">Return_loss(f)≥ $\begin{cases} 22-(20/25.78)f & 0.01\le f < 12.89 \\ 15-(6/25.78)f & 12.89\le f\le 19 \end{cases}$
Where f is the frequency in GHz
Return_loss(f) is the Differential to common-mode return loss at frequency f</td><td>10MHz≤f ≤ 19GHz</td></tr>
<tr><td colspan="2">Common-mode to Common-mode (Input/Output)Return loss S_{CC11}/S_{CC22}</td><td colspan="7">Return_loss(f)≥2dB 0.2≤f≤19
Where f is the frequency in GHz
Return_loss(f) is the Differential to common-mode return loss at frequency f</td><td>10MHz≤f ≤ 19GHz</td></tr>
<tr><td colspan="2">Differential Insertion Loss (S_{DD21} Max.)</td><td colspan="7">(Differential InsertionLoss Max. For TPa to TPb Excluding Test fixture)
<table>
<tr><th>FAWG</th><th>1.25GHz</th><th>2.5GHz</th><th>5.0GHz</th><th>7.0GHz</th><th>10Ghz</th><th>12.89Ghz</th></tr>
<tr><td>30(1m)Max.</td><td>4.5dB</td><td>5.4dB</td><td>6.3dB</td><td>7.5dB</td><td>8.5dB</td><td>10.5dB</td></tr>
<tr><td>30/28(3m) Max.</td><td>7.5dB</td><td>9.5dB</td><td>12.2dB</td><td>14.8dB</td><td>18.0dB</td><td>21.5dB</td></tr>
<tr><td>26(3m)Max.</td><td>5.7dB</td><td>7.2dB</td><td>9.9dB</td><td>11.9dB</td><td>14.1dB</td><td>16.5dB</td></tr>
</table></td><td>10MHz≤f ≤ 19GHz</td></tr>
</table>

	26/25(5m) Max.	7.8dB	10.0dB	13.5dB	16.0dB	19.0dB	22.0dB	
Differential to common-mode Conversion Loss-Differential Insertion Loss(S_{CD21}-S_{DD21})	Conversion _loss(f) – IL(f)≥ $\begin{cases} 10 & 0.01 \le f < 12.89 \\ 27-(29/22)f & 12.89 \le f < 15.7 \end{cases}$ Where f is the frequency in GHz Conversion_loss(f) is the cable assembly differential to common-mode conversion loss IL(f) is the cable assembly insertion loss							10MHz≤f ≤ 19GHz
MDNEXT(multiple disturber near-end crosstalk)	≥26dB @12.89GHz							10MHz≤f ≤ 19GHz

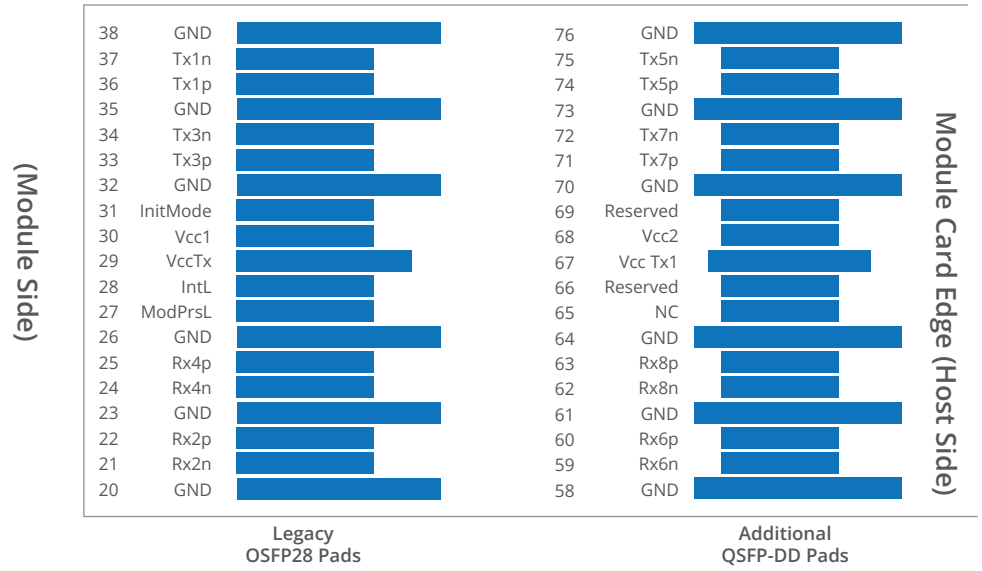
Pin Descriptions@QSFPDD

Pin	Logic	Symbol	Name/Description
1	-	GND	Ground
2	CML-I	Tx2n	Transmitter inverted data input
3	CML-I	Tx2p	Transmitter non-inverted data input
4	-	GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7	-	GND	Ground
8	LVTTL-I	MODSEIL	Module Select
9	LVTTL-I	ResetL	Module Reset
10	-	VCCRx	+3.3V Receiver Power Supply
11	LVCMOS-I/O	SCL	2-wire serial interface clock[2]
12	LVCMOS-I/O	SDA	2-wire serial interface data[2]
13	-	GND	Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16	-	GND	Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver inverted data output
19	-	GND	Ground
20	-	GND	Ground
21	CML-O	Rx2p	Receiver Inverted Data Output
22	CML-O	Rx2n	Receiver Non-Inverted Data Output
23	-	GND	Ground
24	CML-O	RX4p	Receiver Inverted Data Output
25	CML-O	RX4n	Receiver Non-Inverted Data Output

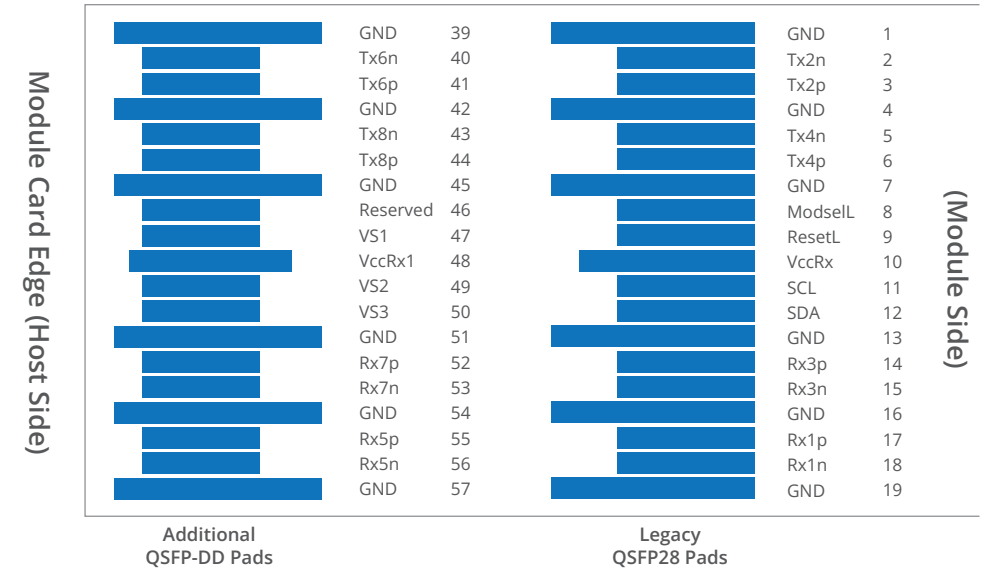
26	-	GND	Ground
27	LVTTL-O	ModPrsL	Module Present
28	LVTTL-O	IntL	Interrupt
29	-	Vcc Tx	+3.3V Transmitter Power Supply
30	-	Vcc1	+3.3V Power Supply
31	LVTTL-I	LPMode	Low Power Mode
32	-	GND	Ground
33	CML-I	Tx3p	Transmitter non-inverted data input
34	CML-I	Tx3n	Transmitter inverted data input
35	-	GND	Ground
36	CML-I	Tx1p	Transmitter non-inverted data input
37	CML-I	Tx1n	Transmitter non-inverted data input
38	-	GND	Ground
39	-	GND	Ground
40	CML-I	Tx6n	Transmitter inverted data input
41	CML-I	Tx6p	Transmitter non-inverted data input
42	-	GND	Ground
43	CML-I	Tx8n	Transmitter inverted data input
44	CML-I	Tx8p	Transmitter non-inverted data input
45	-	GND	Ground
46	-	Reserved	-
47	-	VS1	-
48	-	VCCRx1	+3.3V Power Supply
49	-	VS2	-
50	-	VS3	-
51	-	GND	Ground
52	CML-O	Rx7p	Receiver non-inverted data output
53	CML-O	Rx7n	Receiver inverted data output
54	-	GND	Ground
55	CML-O	Rx5p	Receiver non-inverted data output
56	CML-O	Rx5n	Receiver inverted data output
57	-	GND	Ground
58	-	GND	Ground
59	CML-O	Rx6n	Receiver inverted data output
60	CML-O	Rx6p	Receiver non-inverted data output
61	-	GND	Ground
62	CML-O	Rx8n	Receiver inverted data output
63	CML-O	Rx8p	Receiver non-inverted data output
64	-	GND	Ground

65	-	NC	-
66	-	Reserved	-
67	-	VccTx1	+3.3V Power Supply
68	-	Vcc2	+3.3V Power Supply
69	-	Reserved	-
70	-	GND	Ground
71	CML-I	Rx7p	Transmitter non-inverted data input
72	CML-I	Rx7n	Transmitter inverted data input
73	-	GND	Ground
74	CML-I	Tx5p	Transmitter non-inverted data input
75	CML-I	Tx5n	Transmitter inverted data input
76	-	GND	Ground

Top side viewed from top



Bottom Side Viewed From Bottom



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8	LVTTL-I	ModSelL	Module Select
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16	-	GND	Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Transmitter Inverted DATA in. AC Coupled
19	-	GND	Ground
20	-	GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
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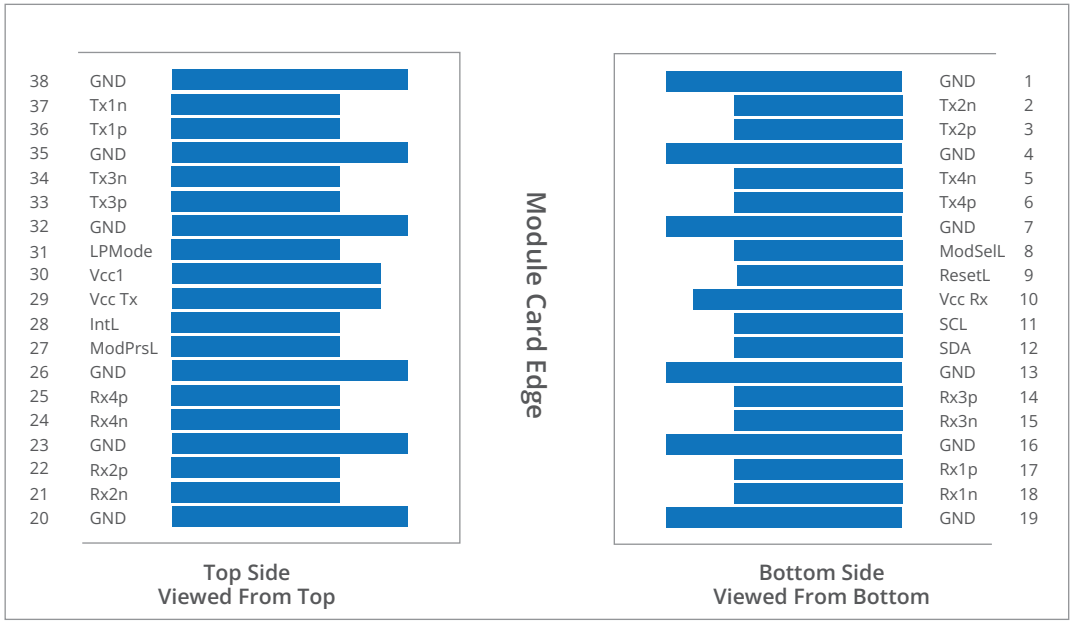
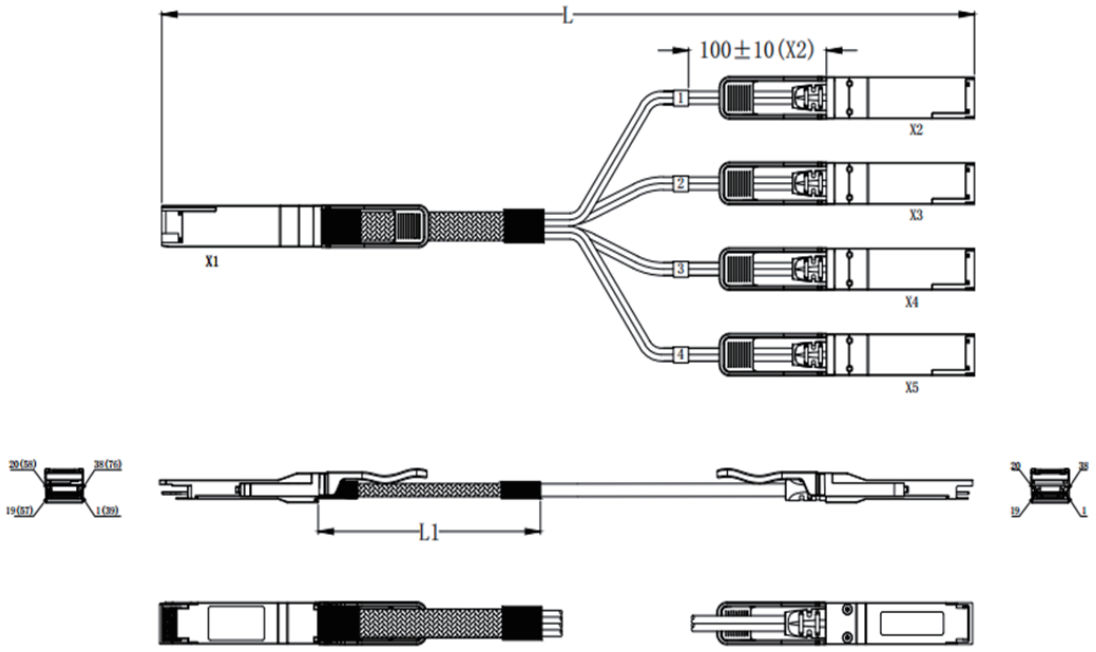
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input

37	CML-I	Tx1n	Transmitter Inverted Data Input
38	-	GND	Ground



Mechanical Specifications



Ordering Information

400G QSFPDD Copper Cable Assemblies, Passive.

P/N	Length	Data Rate	AWG	Length Tolerance
TSD4Q-PCM-01C	1 m	400G	30	+3.5/-3.5 cm
TSD4Q-PCM-02C	2 m	400G	28	+3.5/-3.5 cm
TSD4Q-PCM-03C	2 m	400G	26	+3.5/-3.5 cm