TSQDS-8PC50G-xxM

400G QSFP-DD to 8×50G SFP56 Direct Attach Cable

Description

QSFP-DD to 8xSFP56 passive copper cable assembly feature eight differential copper pairs, providing four data transmission channels at speeds up to 56Gbps (PAM4) per channel, and meets 400G Ethernet. Available in a broad rang of wire gages from 28AWG through 30AWG-this 400G copper cable assembly features low insertion loss and low cross talk.

QSFP-DD to 8xSFP56 uses PAM4 signals for transmission, which doubles the rate. However, there are more stringent requirements for cable insertion loss. For detailed requirements, please see High Speed Characteristics.

Features

- Compatible with IEEE 802.3bj and IEEE 802.3cd
- Supports aggregate data rates of 400Gbps (PAM4)
- Optimized construction to minimize insertion loss and cross talk
- Pull-to-release slide latch design
- 28AWG through 30AWG cable
- Straight and break out assembly configurations available
- Customized cable braid termination limits EMI radiation
- Customizable EEPROM mapping for cable signature
- RoHS compliant

Applications

- Switches, servers and routers
- Data Center networks
- Storage area networks
- High performance computing
- Telecommunication and wireless infrastructure
- Medical diagnostics and networking
- Test and measurement equipment

Recommended Operation Condition

Parameters	Symbol	Min.	Max.	Unit
Operating Case Temperature	Topc	0	70	degC
Storage Temperature	Tst	-40	85	degC
Relative Humidity (non-condensation)	RS	35	60	%
Supply Voltage	Vcc3	3.135	3.465	V
Voltage on LVTTL Input	Vilvttl	-0.3	Vcc3+0.2	V
Power Supply Current	Icc3	-	15	mA
Total Power Consumption	Pd	-	0.05	W

Notes:
Stress or conditions exceed the above range may cause permanent damage to the device.
This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not applied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

High Speed Characteristics

Parameter	Symbol	Min.	Typical	Max.	Units	Notes
Differential Impedance	TDR	90	100	110	Ω	-
Insertion Loss	SDD21	-16.06	-	-	dB	At 13.28 GHz
Differential Input Return Loss	SDD11 SDD22	-	-	See 1	dB	At 0.05 to 4.1 GHz
		-	-	See 2		At 4.1 to 19 GHz
Common Mode Output Return Loss	SCC11	-	-	-2	dB	At 0.2 to 19 GHz
Differential to Common-mode Return Lss	SCD11 SCD22	-	-	See 3	dB	At 0.01 to 12.89 GHz At 12.89 to 19 GHz
		-	-	See 4		
Differential to Common-mode Conversion Loss	SCD21-IL	-	-	-10	dB	At 0.01 to 12.89 GHz
		-	-	See 5		At 12.89 to 15.7 GHz
		-	-	-6.3		At 15.7 to 19 GHz
Channel Operating Margin	COM	-	-	-3	dB	-

Notes:
[1] Reflection Coefficient given by equation SDD11(dB) < -16.5 + 2 × SQRT(f), with f in GHz
[2] Reflection Coefficient given by equation SDD11(dB) < -10.66 + 14 × log10(f/5.5), with f in GHz
[3] Reflection Coefficient given by equation SCD11(dB) < -22 + (20/25.78)*f, with f in GHz
[4] Reflection Coefficient given by equation SCD11(dB) < -15 + (6/25.78)*f, with f in GHz
[5] Reflection Coefficient given by equation SCD21(dB) < -27 + (29/22)*f, with f in GHz

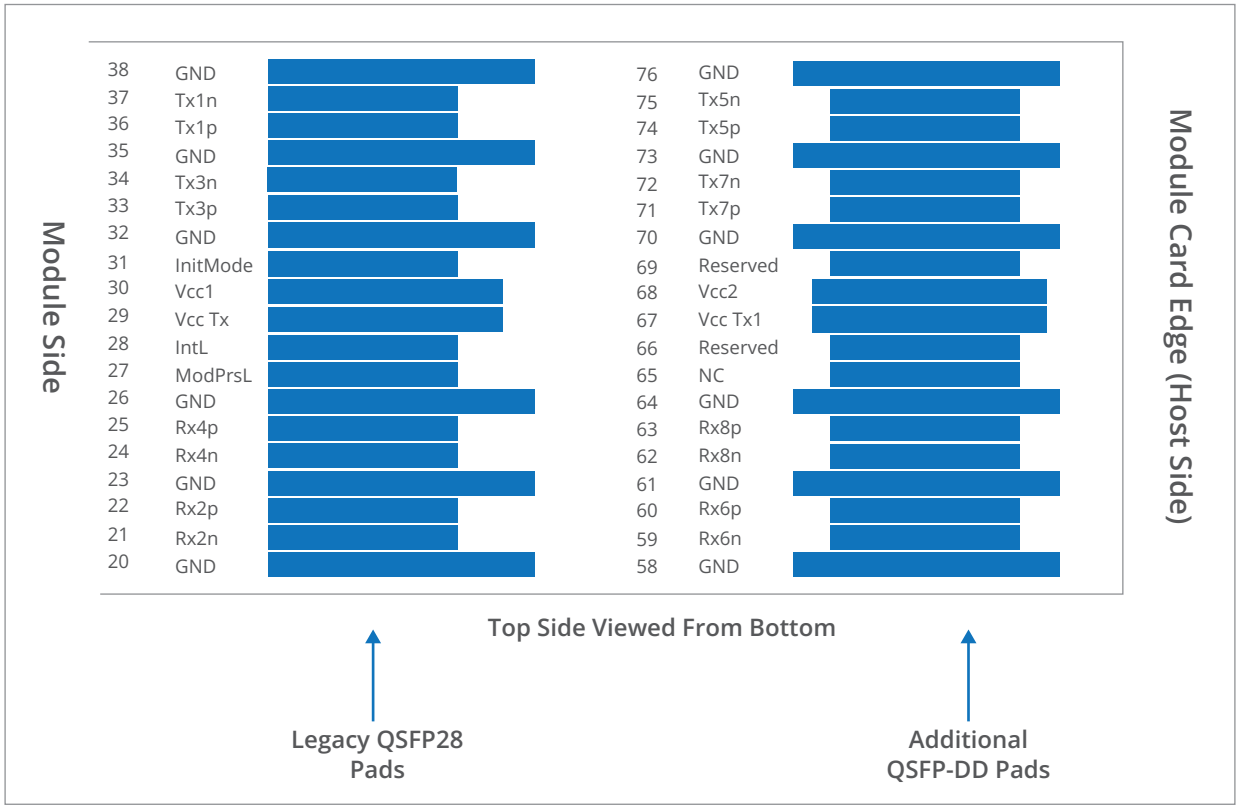
QSFP-DD Pin Definition

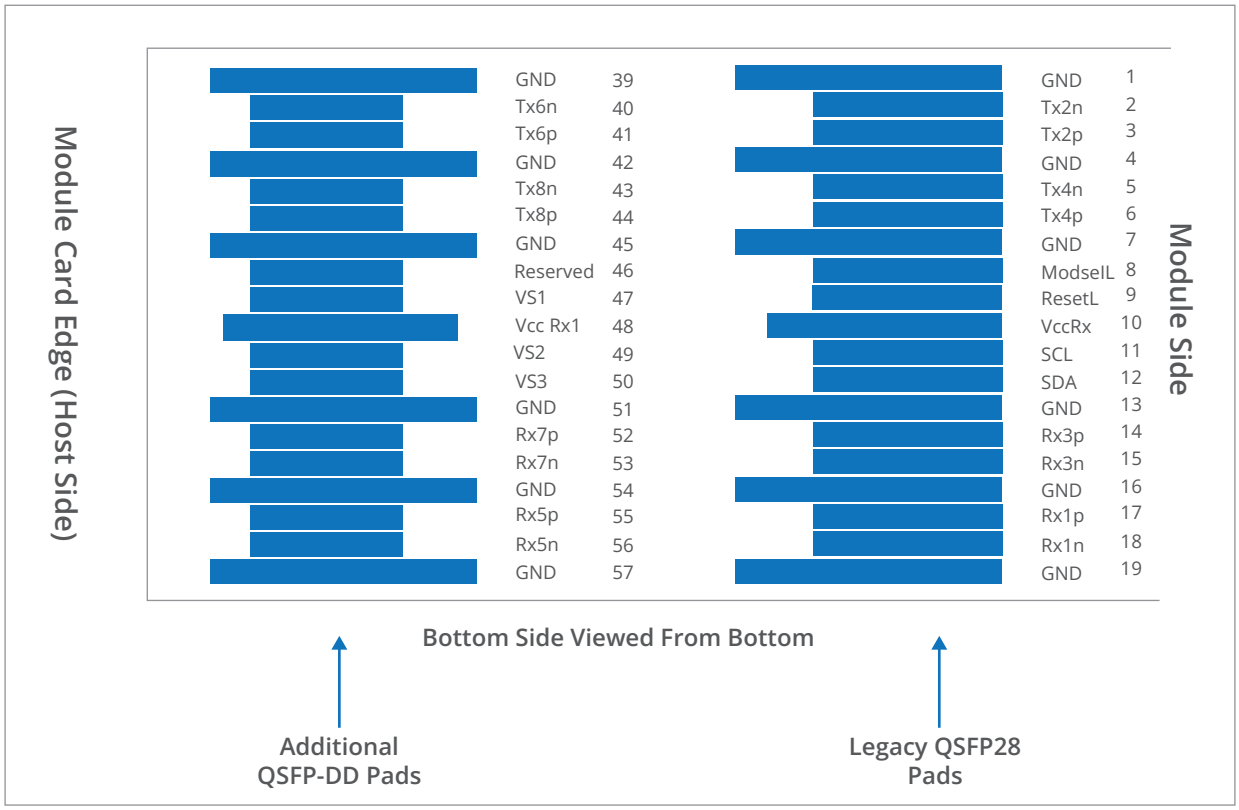
Pin	Logic	Symbol	Name/Description
1	-	GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input
4	-	GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input

6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7	-	GND	Ground
8	LVTTL-I	ModSelL	Module Select
9	LVTTL-I	ResetL	Module Reset
10	-	Vcc Rx	+3.3V Power supply receiver
11	LVCMOS-I/O	SCL	2-wire serial interface clock
12	LVCMOS-I/O	SDA	2-wire serial interface data
13	-	GND	Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16	-	GND	Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Transmitter Inverted DATA in. AC Coupled
19	-	GND	Ground
20	-	GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-Inverted Data Output
23	-	GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-Inverted Data Output
26	-	GND	Ground
27	LVTTL-O	ModPrsL	Module Present
28	LVTTL-O	IntL	Interrupt
29	-	Vcc Tx	+3.3V Power supply transmitter
30	-	Vcc1	+3.3V Power Supply
31	LVTTL-I	LPMode	Low Power Mode
32	-	GND	Ground
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35	-	GND	Ground
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38	-	GND	Ground
39	-	GND	Ground
40	CML-I	Tx6n	Transmitter Inverted Data Input
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input
42	-	GND	Ground
43	CML-I	Tx8n	Transmitter Inverted Data Input

44	CML-I	Tx8p	Transmitter Non-Inverted Data Input
45	-	GND	Ground
46	-	Reserved	-
47	-	VS1	-
48	-	Vcc Rx1	+3.3V Power supply receiver
49	-	VS2	-
50	-	VS3	-
51	-	GND	Ground
52	CML-O	Rx7p	Receiver Non-Inverted Data Output
53	CML-O	Rx7n	Receiver Inverted Data Output
54	-	GND	Ground
55	CML-O	Rx5p	Receiver Non-Inverted Data Output
56	CML-O	Rx5n	Receiver Inverted Data Output
57	-	GND	Ground
58	-	GND	Ground
59	CML-O	Rx6n	Receiver Inverted Data Output
60	CML-O	Rx6p	Receiver Non-Inverted Data Output
61	-	GND	Ground
62	CML-O	Rx8n	Receiver Non-Inverted Data Output
63	CML-O	Rx8p	Receiver Non-Inverted Data Output
64	-	GND	Ground
65	-	NC	-
66	-	Reserved	-
67	-	Vcc Tx1	+3.3V Power supply
68	-	Vcc2	+3.3V Power supply
69	-	Reserved	-
70	-	GND	Ground
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input
72	CML-I	Tx7n	Transmitter Inverted Data Input
73	-	GND	Ground
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input
75	CML-I	Tx5n	Transmitter Inverted Data Input
76	-	GND	Ground

Pin Definition





SFP 56 Pin Descriptions

Pin	Symbol	Name/Description
1	VeeT [1]	Transmitter Ground
2	Tx_FAULT [2]	Not used
3	Tx_DIS [3]	Not used
4	SDA [2]	2-wire Serial Interface Data Line
5	SCL [2]	2-wire Serial Interface Clock Line
6	MOD_ABS [4]	Module Absent. Grounded within the module
7	RS0 [5]	Not used
8	RX_LOS [2]	Loss of Signal indication. Logic 0 indicates normal operation
9	RS1 [5]	Not used
10	VeeR [1]	Receiver Ground
11	VeeR [1]	Receiver Ground
12	RD-	Receiver Inverted DATA out. AC Coupled
13	RD+	Receiver DATA out. AC Coupled
14	VeeR [1]	Receiver Ground
15	VccR	Receiver Power Supply
16	VccT	Transmitter Power Supply
17	VeeT [1]	Transmitter Ground
18	TD+	Transmitter DATA in. AC Coupled
19	TD-	Transmitter Inverted DATA in. AC Coupled
20	VeeT [1]	Transmitter Ground

Notes:

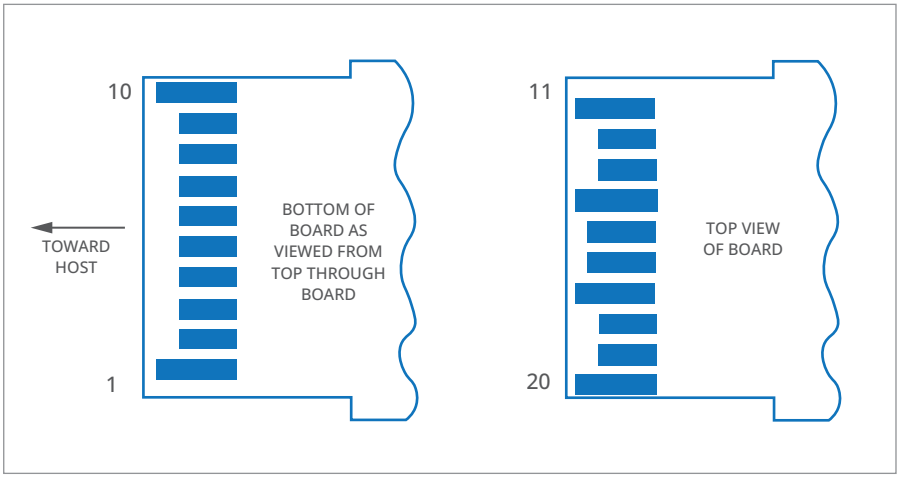
[1] Module circuit ground is isolated from module chassis ground within the module.

[2] Should be pulled up with 4.7k – 10k ohms on host board to a voltage between 3.15Vand 3.6V.

[3] Tx_Disable is an input contact with a 4.7 kΩ to 10 kΩ pullup to VccT inside the module.

[4] Mod_ABS is connected to VeeT or VeeR in the SFP+ module. The host may pull this contact up to Vcc_Host with a resistor in the range 4.7 kΩ to10 kΩ.Mod_ABS is asserted "High" when the SFP+ module is physically absent from a host slot.

[5] RS0 and RS1 are module inputs and are pulled low to VeeT with > 30 kΩ resistors in the module.



Ordering Information

400G QSFP-DD 8x50G SFP56 Copper Breakout Cable Assemblies, Passive.

P/N	Length	Data Rate	AWG	Length Tolerance
TSQDQ-8PC2HG-01M	1 m	400G	30	+3.5/-3.5 cm
TSQDQ-8PC2HG-02M	2 m	400G	28	+3.5/-3.5 cm
TSQDQ-8PC2HG-03M	3 m	400G	28	+4/-4 cm